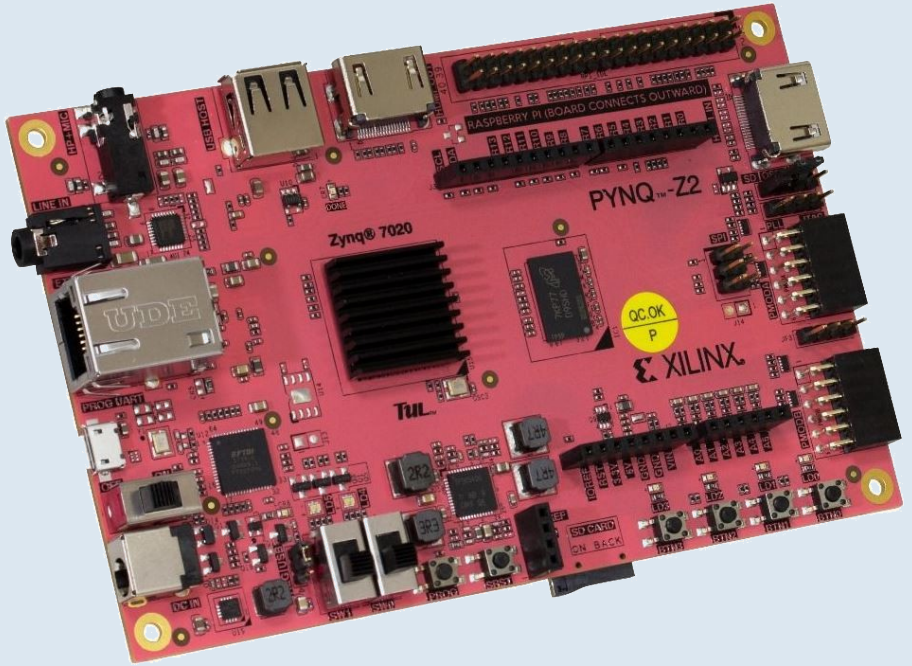
Part 3: The Pynq-Z2 SoC

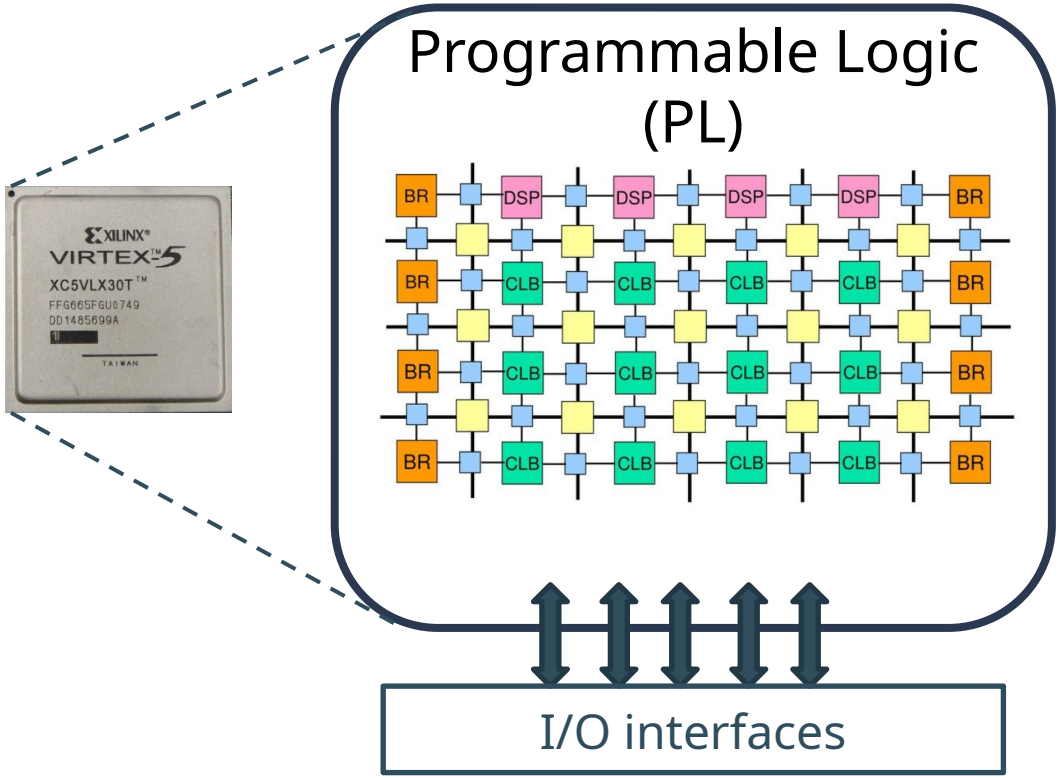


Xilinx ‘Traditional’ FPGAs

- Two main families: Virtex vs. Spartan (currently Artix)
- Technology advances = devices with more resources (logic cells, BRAM, DSP, …)

Xilinx FPGA Families

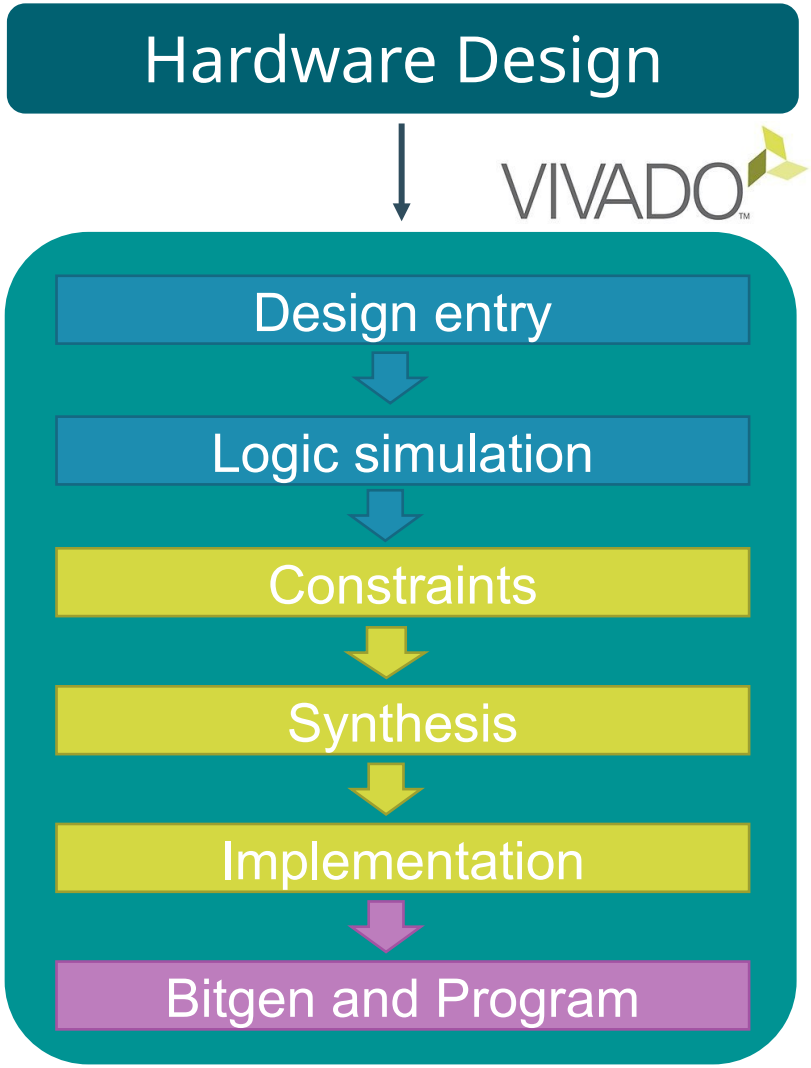
Technology	Low-cost	High-performance
220 nm		Virtex
180 nm	Spartan II, Spartan IIE	
120/150 nm		Virtex II, Virtex II Pro
90 nm	Spartan 3	Virtex 4
65 nm		Virtex 5
45 nm	**Spartan 6**	
40 nm		Virtex 6
28 nm	Artix 7	Virtex 7



Xilinx ‘Traditional’ FPGAs

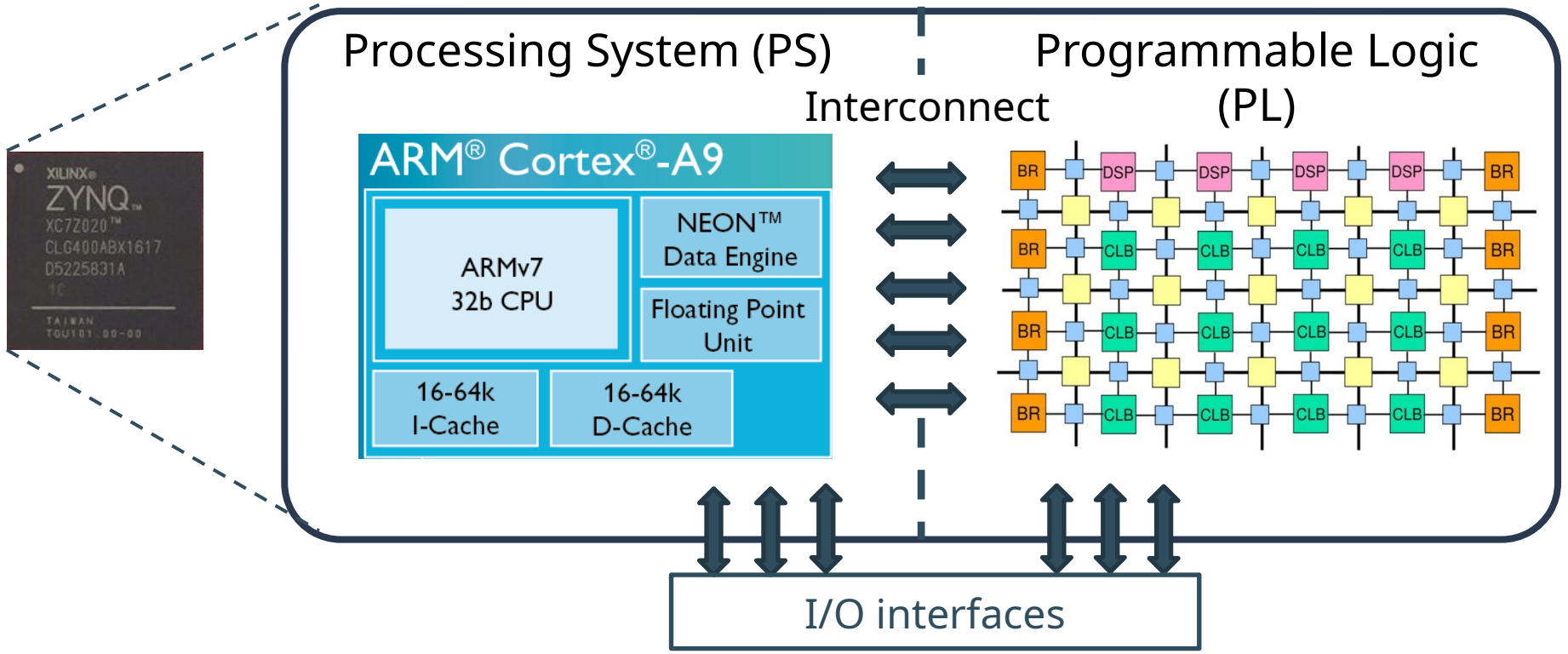
- Programming model: FPGA-only
- Platforms targeted to hardware design
- Development tools: Vivado (formely ISE)

- Note: hardware/software co-design still possible
- Soft core: CPU implemented on the PL
  - → Proprietary: MicroBlaze, PicoBlaze (Xilinx)
  - → Open-source: 8051, AVR clones, …
  - → Dedicated: custom instruction set



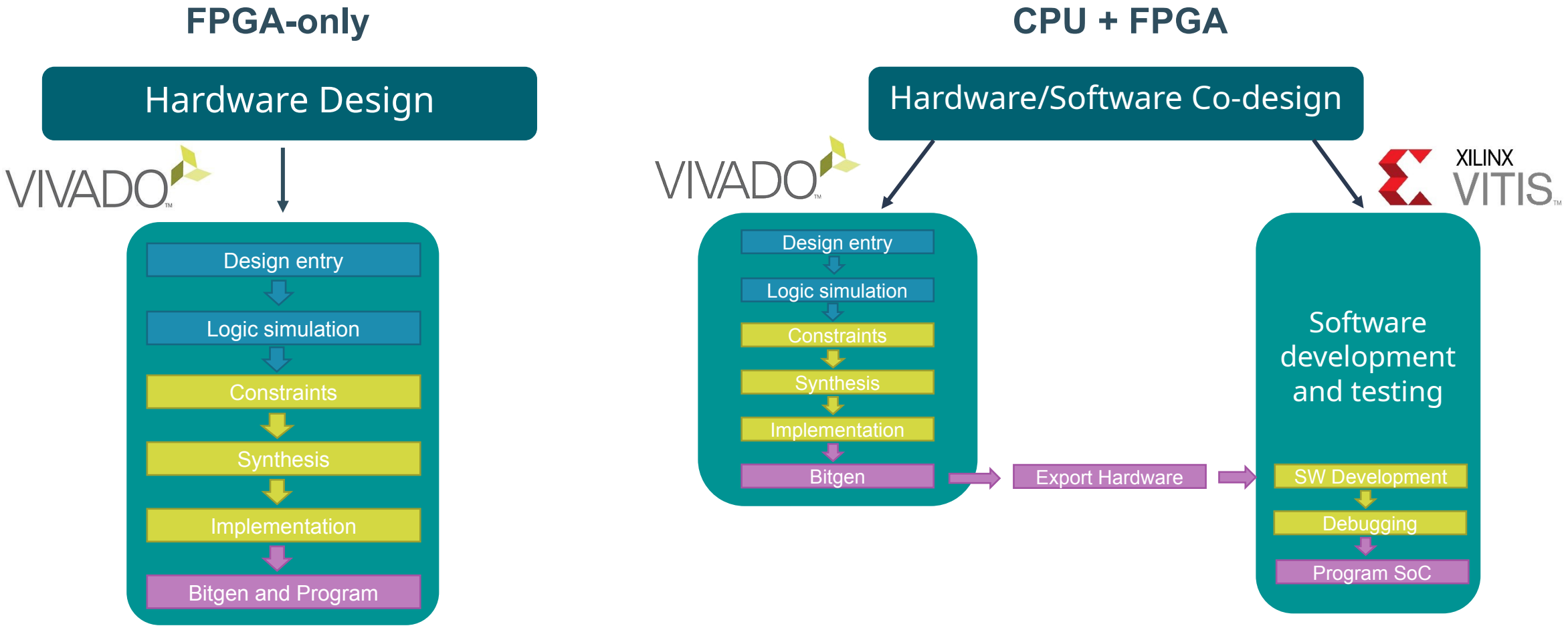
Xilinx Zynq-7000 series

- Introduced in 2011: System-on-Chip (SoC) architecture
- Hard core processor (ARM Cortex-A9) : Processing System (PS)
- FPGA configurable logic (Artix-7 / Kintex-7): Programmable Logic (PL)



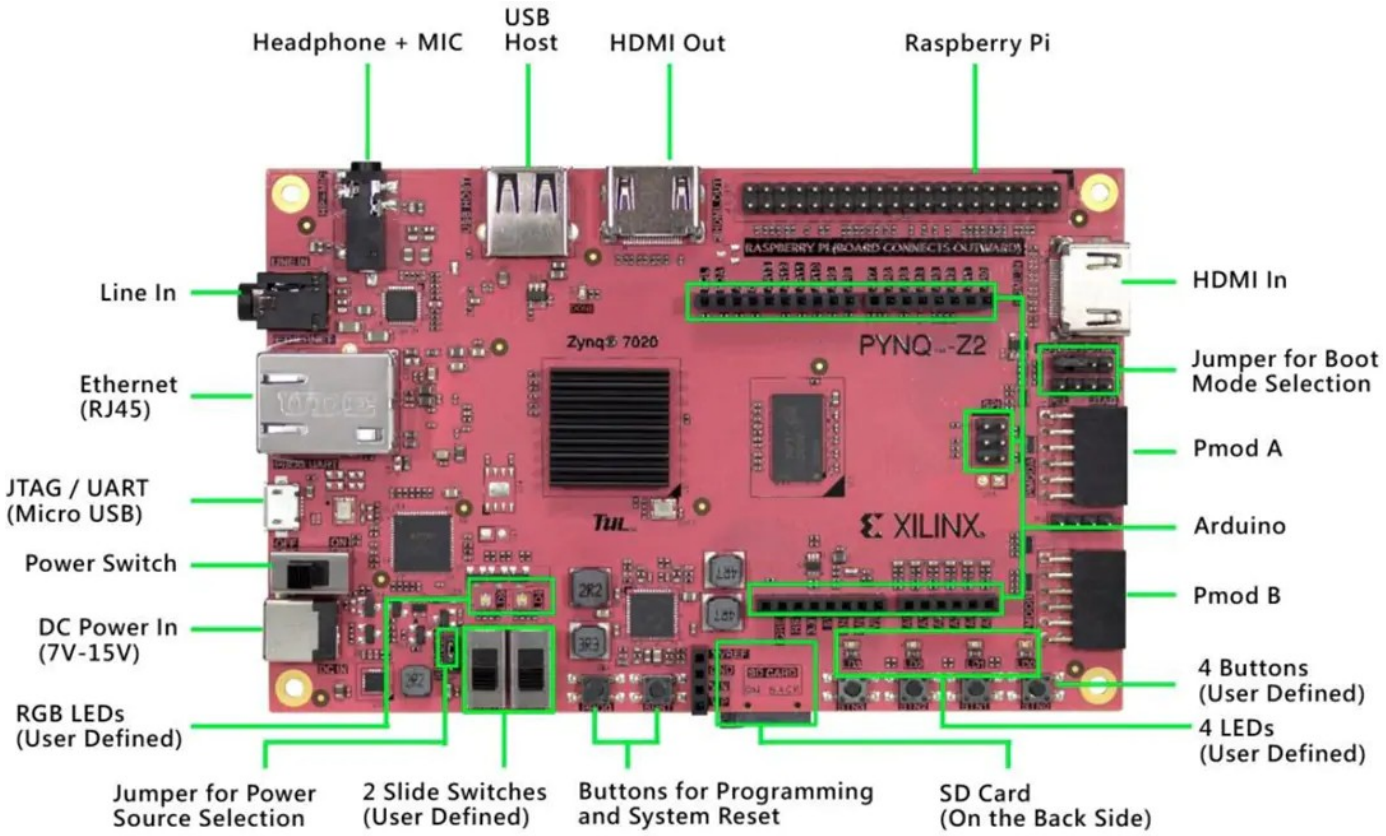
Xilinx Zynq-7000 series

- Supports two programming modes



Pynq-Z2 Board

- Evaluation board designed around the Zynq-7000 SoC
- More specifically: Zynq-7020 SoC (cost-optimized family)

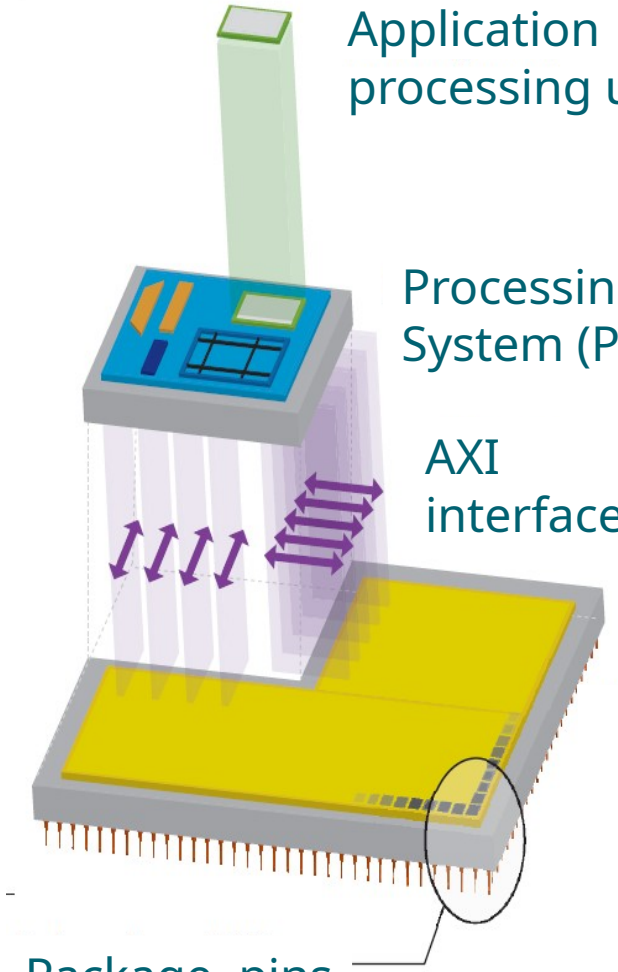


Zynq 7020 SoC – Specifications

Zynq®-7000 SoC Family

		Cost-Optimized Devices						Mid-Range Devices			
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System (PS)	Processor Core	Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz			Dual-Core ARM Cortex-A9 MPCore Up to 866MHz			Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1]			
	Processor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor									
	L1 Cache	32KB Instruction, 32KB Data per processor									
	L2 Cache	512KB									
	On-Chip Memory	256KB									
	External Memory Support[2]	DDR3, DDR3L, DDR2, LPDDR2									
	External Static Memory Support[2]	2x Quad-SPI, NAND, NOR									
	DMA Channels	8 (4 dedicated to PL)									
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO									
	Peripherals w/ built-in DMA[2]	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO									
	Security[3]	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot									
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts									
Programmable Logic (PL)	7 Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7
	Logic Cells	23K	55K	65K	28K	74K	85K	125K	275K	350K	444K
	Look-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	1.8Mb (50)	2.5Mb (72)	3.8Mb (107)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.2Mb (545)	26.5Mb (755)
	DSP Slices	66	120	170	80	160	220	400	900	900	2,020
	PCI Express®	—	Gen2 x4	—	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC[2]	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs									
	Security[3]	AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config									
	Speed Grades: Commercial	-1			-1			-1			-1
	Speed Grades: Extended	-2			-2,-3			-2,-3			-2
	Speed Grades: Industrial	-1, -2			-1, -2, -1L			-1, -2, -2L			-1, -2, -2L

Zynq 7020 SoC – Block Diagram



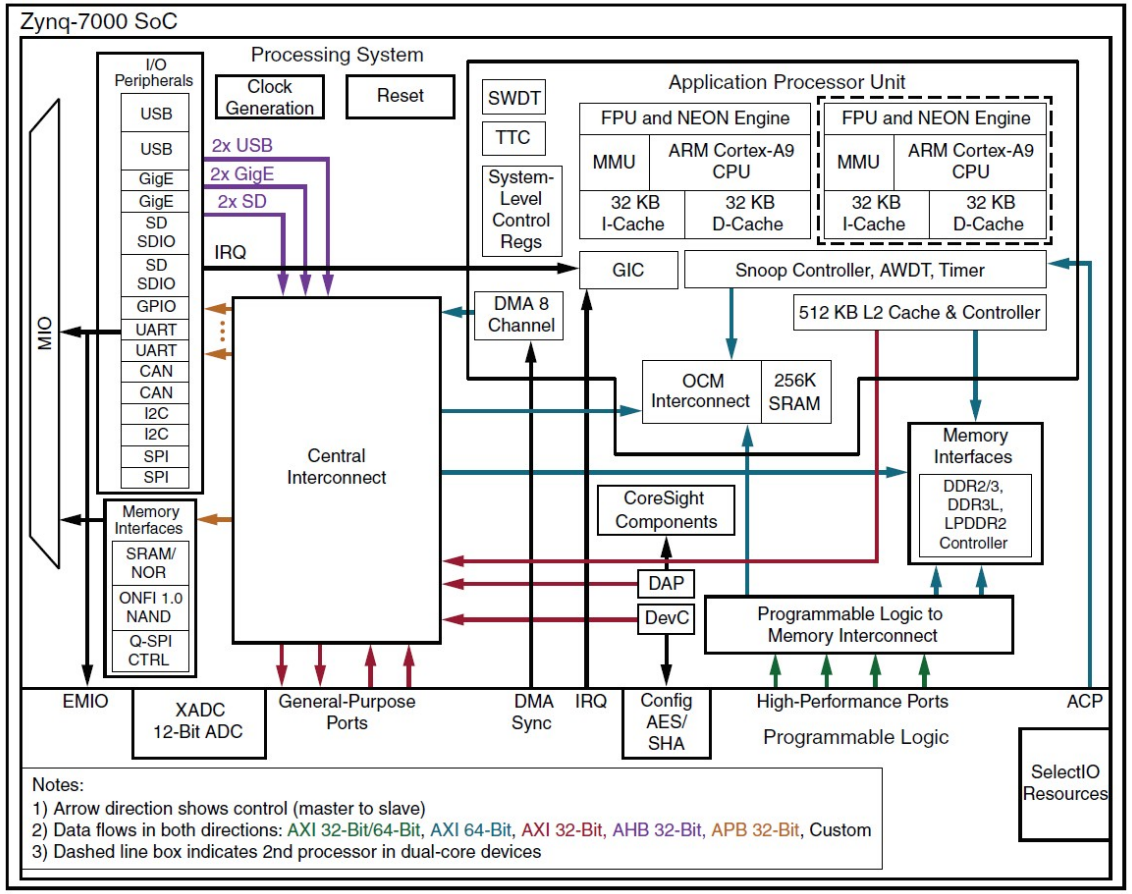
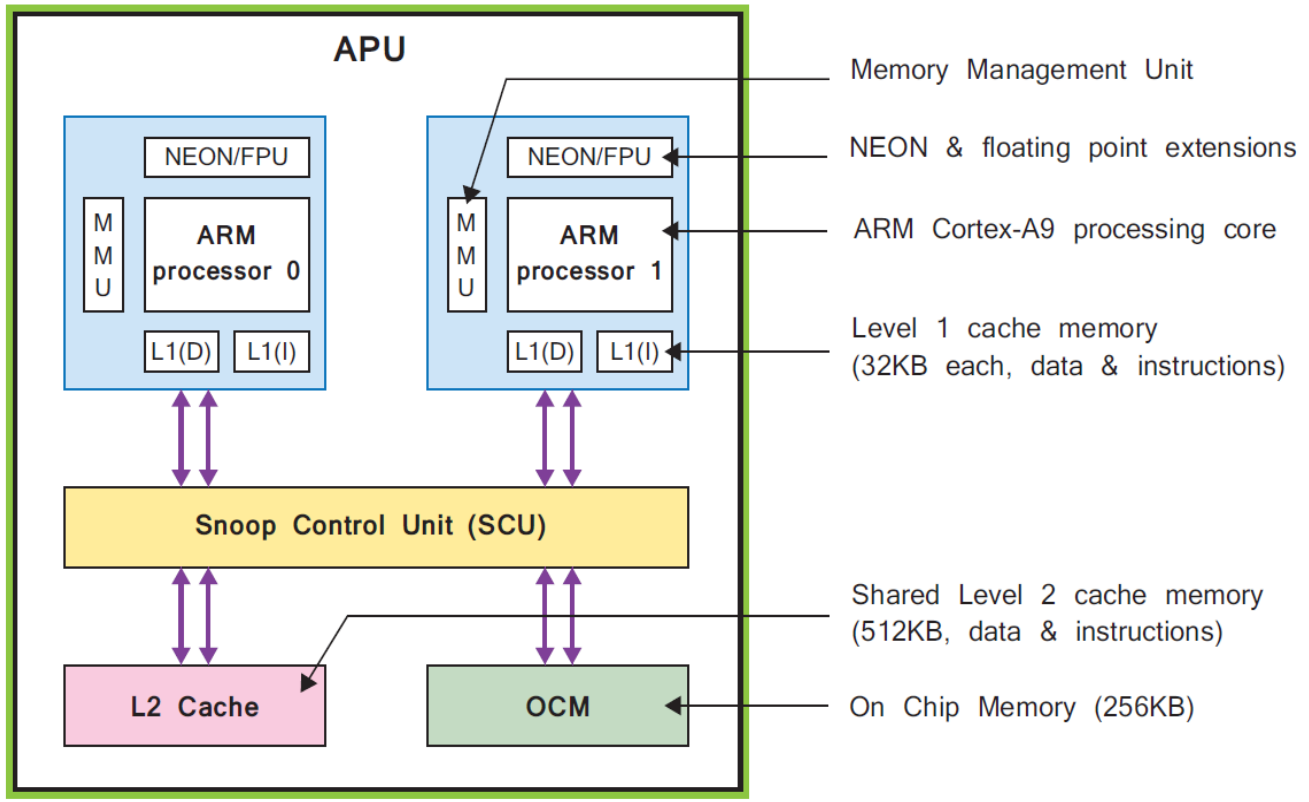


Figure 1: **Architectural Overview**

Zynq 7020 SoC – Application Processing Unit (APU)

(simplified view)

- Two ARM processor cores
- Each with associated computational units
  - NEON SIMD extension
  - L1 cache memory
- Snoop Control Unit bridges ARM cores with L2 cache and On-Chip Memory
- Also responsible for interfacing with the PL (not shown here)



Zynq 7020 SoC – Processing System (PS)

(simplified view)

- Extends the APU with peripherals and external interfaces
- Central interconnect manages communication within the PS
  - Direct interfaces : Multiplexed Input/Output (MIO)
  - Memory interfaces
  - Extended interfaces : Extended MIO (through PL)
- Other interesting blocks:
  - DMA : Direct Memory Access
  - Global Interrupt Controller
  - Clock / Reset generation

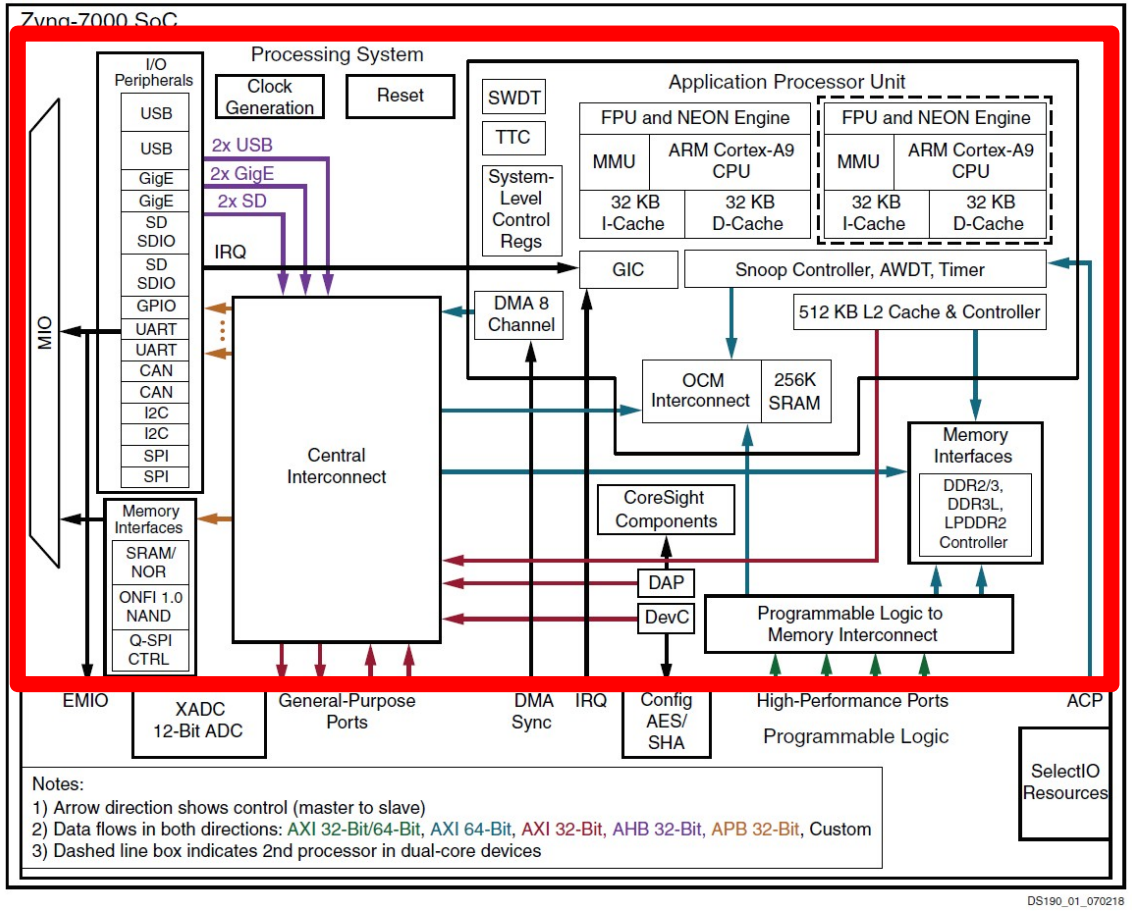
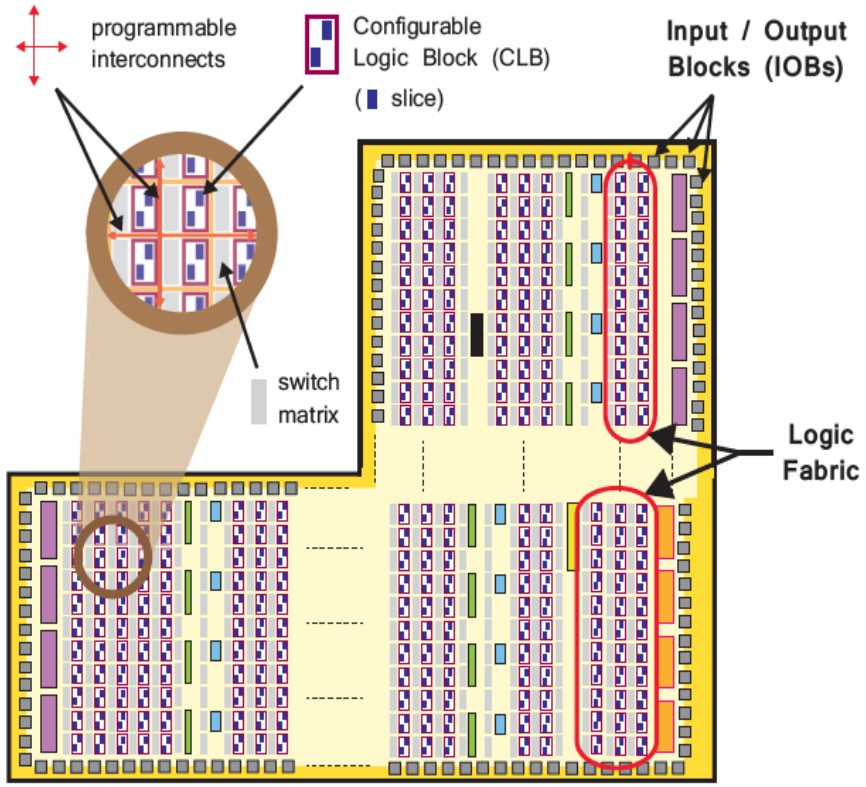


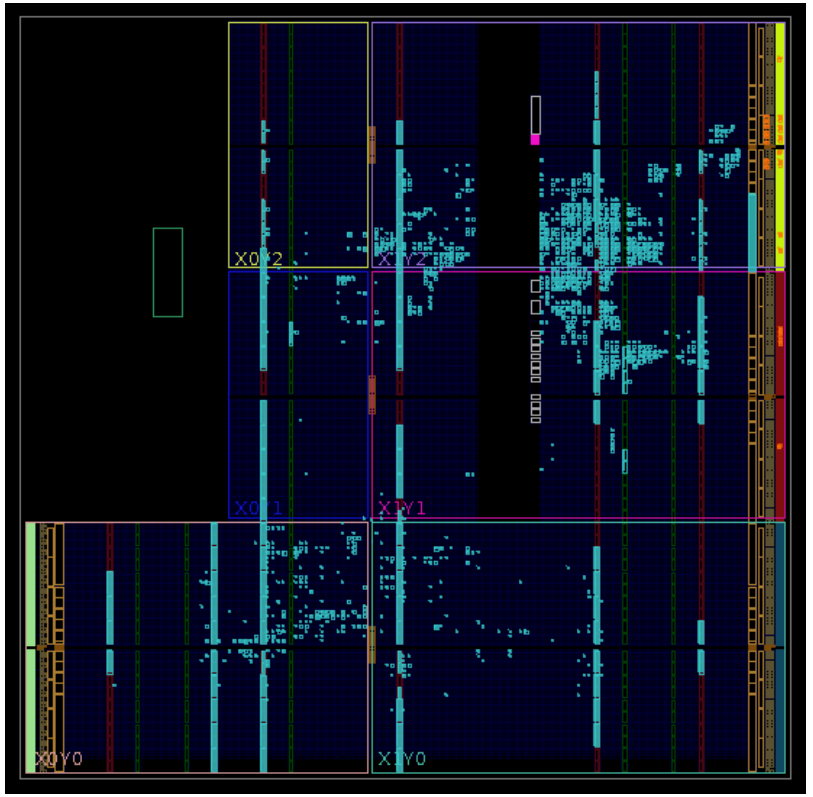
Figure 1: **Architectural Overview**

Zynq 7020 SoC – Programmable Logic (PL)

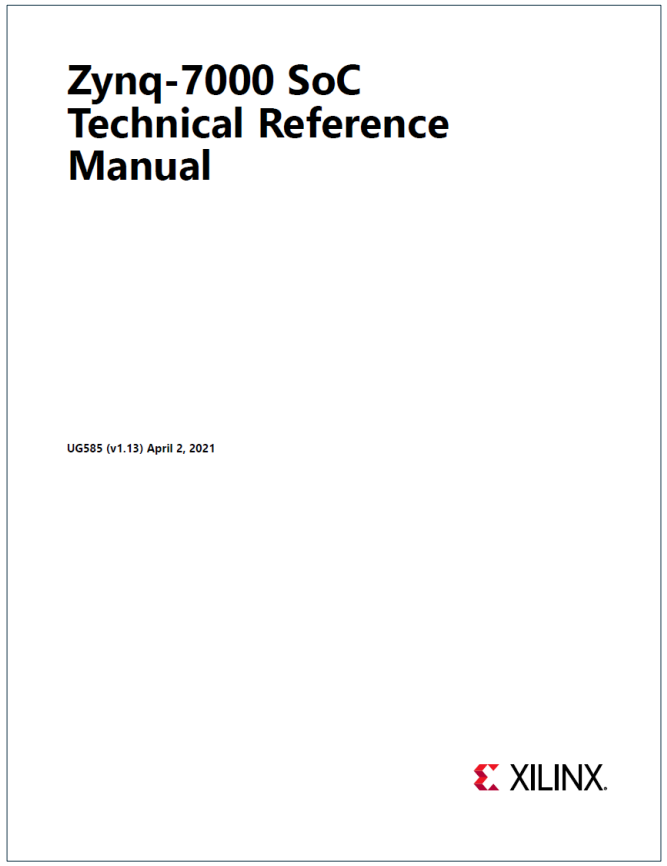
(simplified view)



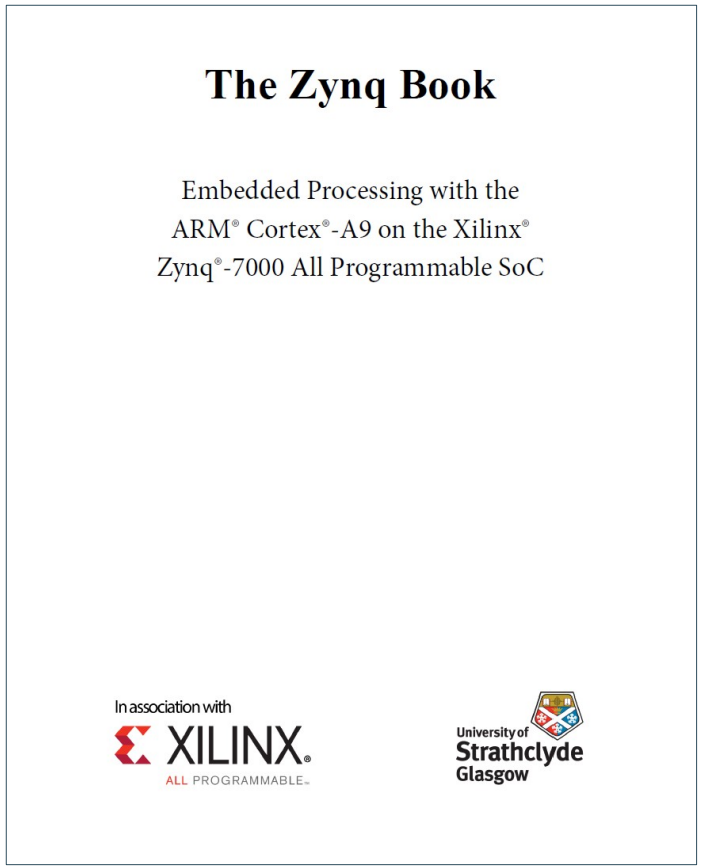
Visible in Vivado after implementation
("Window" → "Device")



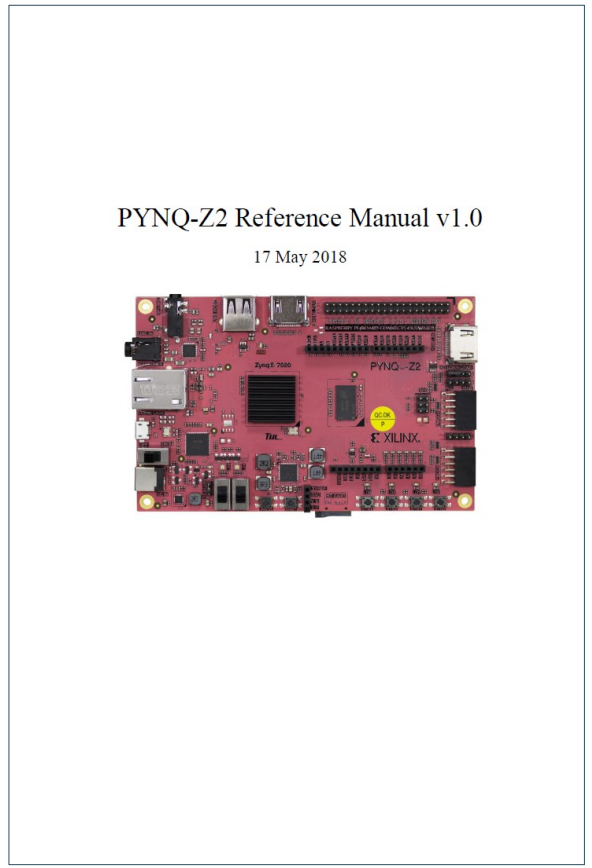
Useful Resources



*"The Bible" : **all** information is in there (1800 pages)*



Most accessible resource, recommended reading



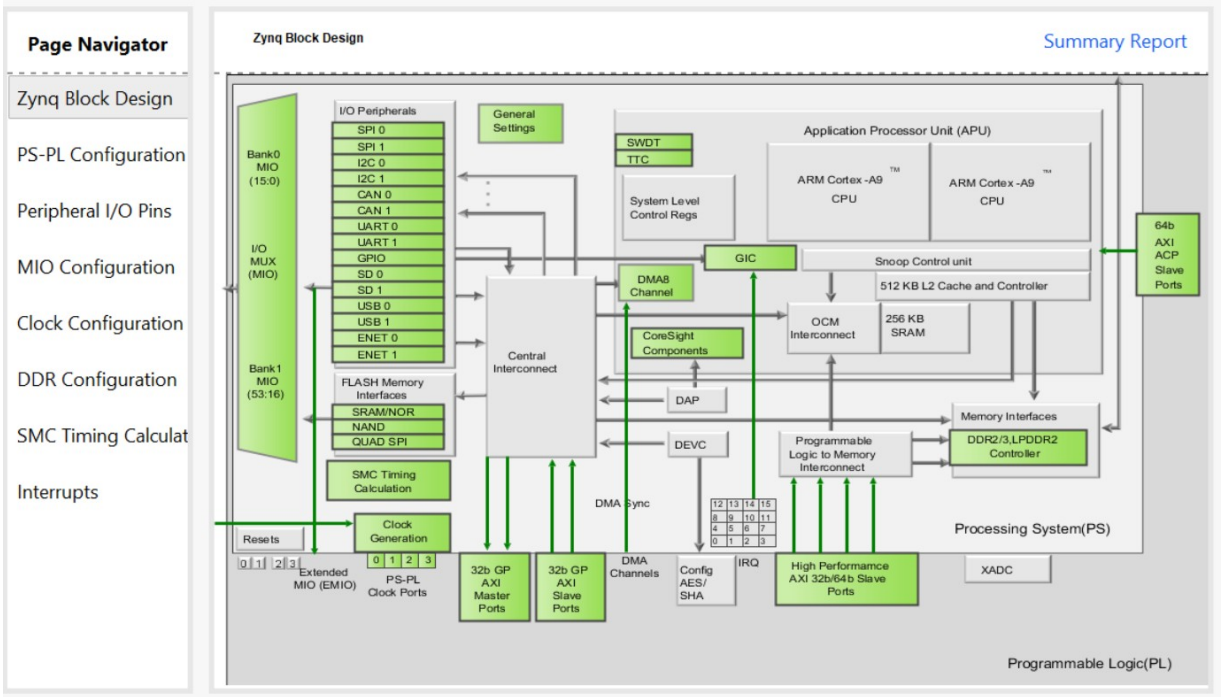
Mapping ZYNQ to Pynq-Z2 (important for PS customization and I/O interfacing)

Enabling CPU + FPGA flow

- Need to add **ZYNQ7 Processing System** in Vivado (IP block)
- This effectively *instantiates* the PS in our hardware design
- There is a pre-defined configuration for the Pynq-Z2 (after *Run Block Automation*)
- Double-clicking on the block allows to configure the parameters of the PS



- Default configuration:
  - 100 MHz clock
  - Synchronous reset
  - Built-in UART port
  - DDR memory



Way Forward

Hands-On: Vivado/Vitis Flow (Hello World + Debug)

- Objective: understand ARM+FPGA design flow using Vitis and Vivado

  Follow the embedded software Getting_started tutorial here :
  https://github.com/Xilinx/Vitis-Tutorials/tree/2024.1/Embedded_Software/Getting_Started

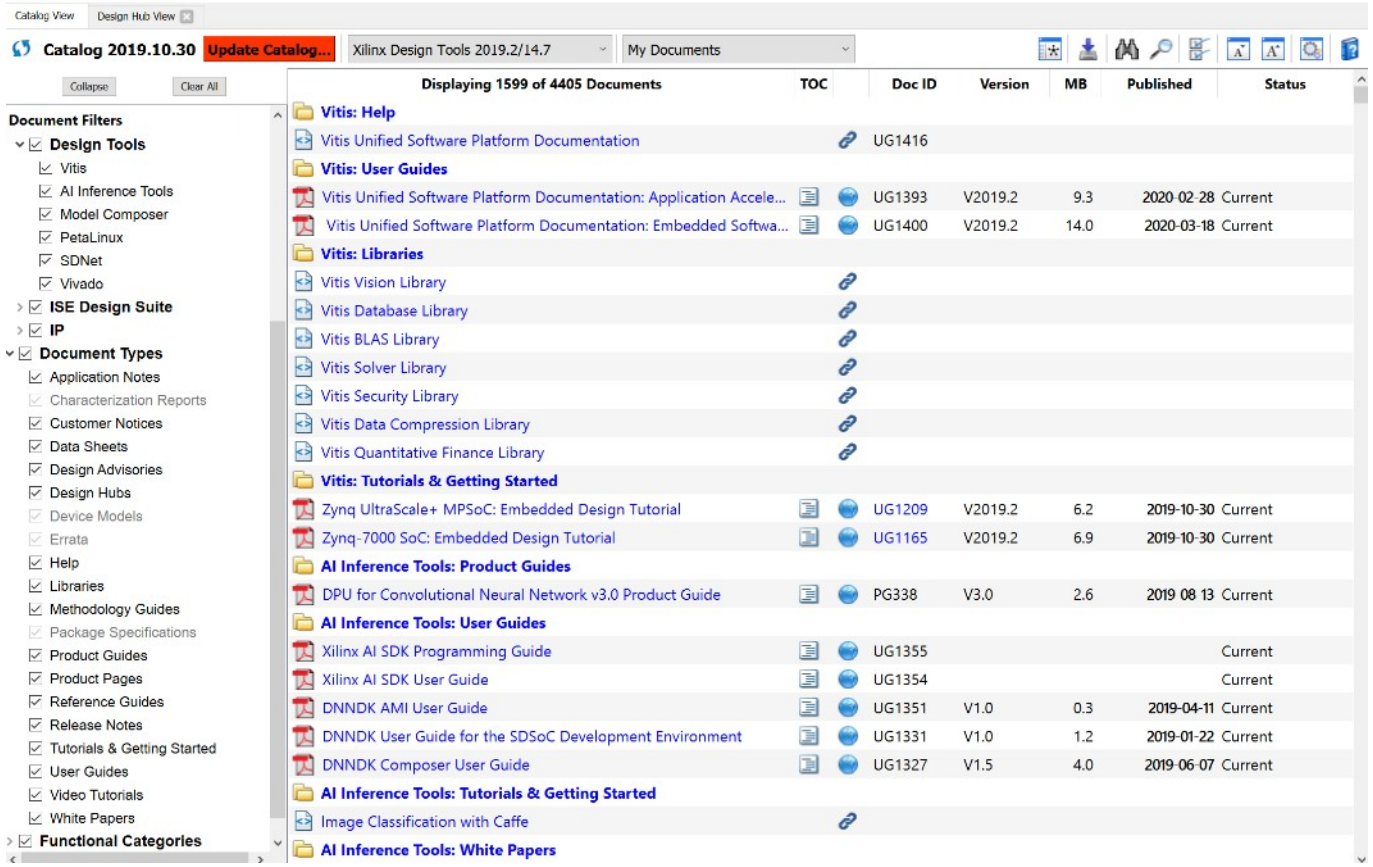
- Some information about Platform creation (ZynqMP, Kria KV260) can be found here:
  https://github.com/Xilinx/Vitis-Tutorials/tree/2024.1/Vitis_Platform_Creation
  This does not contain Zynq information, ZynqMP has a bit more to configure like Power and Security Management (pmufw.elf) and ARM Trusted Firmware (bl31.elf) which do not exist on Zynq

All of the Vitis tutorials can be found at https://github.com/Xilinx/Vitis-Tutorials?tab=readme-ov-file#tutorials this contains many parts we will not cover in this course (Alveo Data Center, HLS). But feel free to be a rebel!

Very useful resource: DocNav



- Xilinx provides extensive documentation for devices and toolchains
  - In-depth explanation of Vivado processes: simulation, synthesis, implementation, …
  - Dedicated tutorials for specific devices: for instance Zynq-7000



- Documents change from Vivado version to version, so it is important to have the right one
- DocNav is a good resource to access documentation